

KAF- 1401E

1320 (H) x 1035 (V) Pixel

Enhanced Response

Full-Frame CCD Image Sensor

Performance Specification

Eastman Kodak Company

Microelectronics Technology Division

Rochester, New York 14650-2010

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1.1 Features

- 1.4 Million Pixel Area CCD
- 1320H x 1034V Pixels
- Transparent Gate True Two Phase Technology (Enhanced Spectral Response)
- 6.8 x 6.8mm Pixels
- 8.9 mm H x 7.04mm V Photosensitive Area
- 100% Fill Factor
- High Output Sensitivity (11mV/e-)
- Low Dark Current (<10pA/cm² @ 25°C)

1.2 Description

The KAF-1401E is a high performance monochrome area CCD (charge-coupled device) image sensor with 1320H x 1035V photoactive pixels designed for a wide range of image sensing applications in the 0.4nm to 1.0nm wavelength band. Typical applications include military, scientific, and industrial imaging. A 70dB dynamic range is possible operating at room temperature.

The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400nm, compared to a front side illuminated standard poly silicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths.

The photoactive area is 8.98mm x 7.04mm and is housed in a 68-pin, pin grid array ceramic package with 0.1" pin spacing.

The sensor consists of 1320 parallel (vertical) CCD shift registers each 1035 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The parallel (vertical) CCD registers transfer the image one line at a time into a single 1348 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo generated charge to a voltage for each pixel.

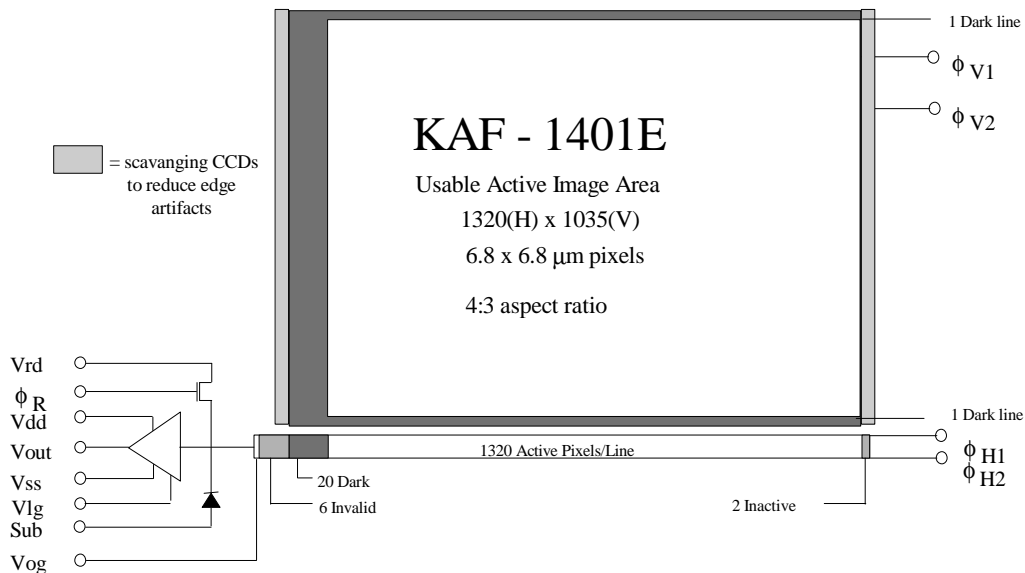


Figure 1 – Functional Block Diagram



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1.3 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the Φ_{V1} and Φ_{V2} register clocks are held at a constant (low) level.

See Figure 5. - Timing Diagrams.

1.4 Charge Transport

Referring again to Figure 5 - Timing Diagrams, the integrated charge from each photogate is transported to the output using a two step process. Each line (row) of charge is first transported from the vertical CCD's to the horizontal CCD register using the Φ_{V1} and Φ_{V2} register clocks. The horizontal CCD is presented a new line on the falling edge of Φ_{V2} while Φ_{H1} is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the Φ_{H1} and Φ_{H2} pins in a complementary fashion. On each falling edge of Φ_{H2} a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

1.5 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge

placed on FD. Once the signal has been sampled by the system electronics, the reset gate (Φ_R) is clocked to remove the signal and FD is reset to the potential applied by Vrd. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device - see Figure 4.

1.6 Dark Reference Pixels

At the beginning of each line are 20 light shielded pixels. There is also 1 full dark line at the start of every frame and 1 full dark line at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, (including the 2 full dark lines and one column at end of each line), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

1.7 Dummy Pixels

Within the horizontal shift register are 6 leading additional pixels which are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions. There are two more dummy pixels at the end of each line.

There are several columns of dummy vertical CCD at the adjacent to the photo active vertical CCD that act to scavenge unwanted stray signal away from the imaging area. These columns are not connected to the horizontal register so their presence does not have to be taken into account when clocking out each line. They transfer their charge in a direction opposite of the photo-active columns and the charge is removed through a connection to Vdd.



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2.1 Package Configuration

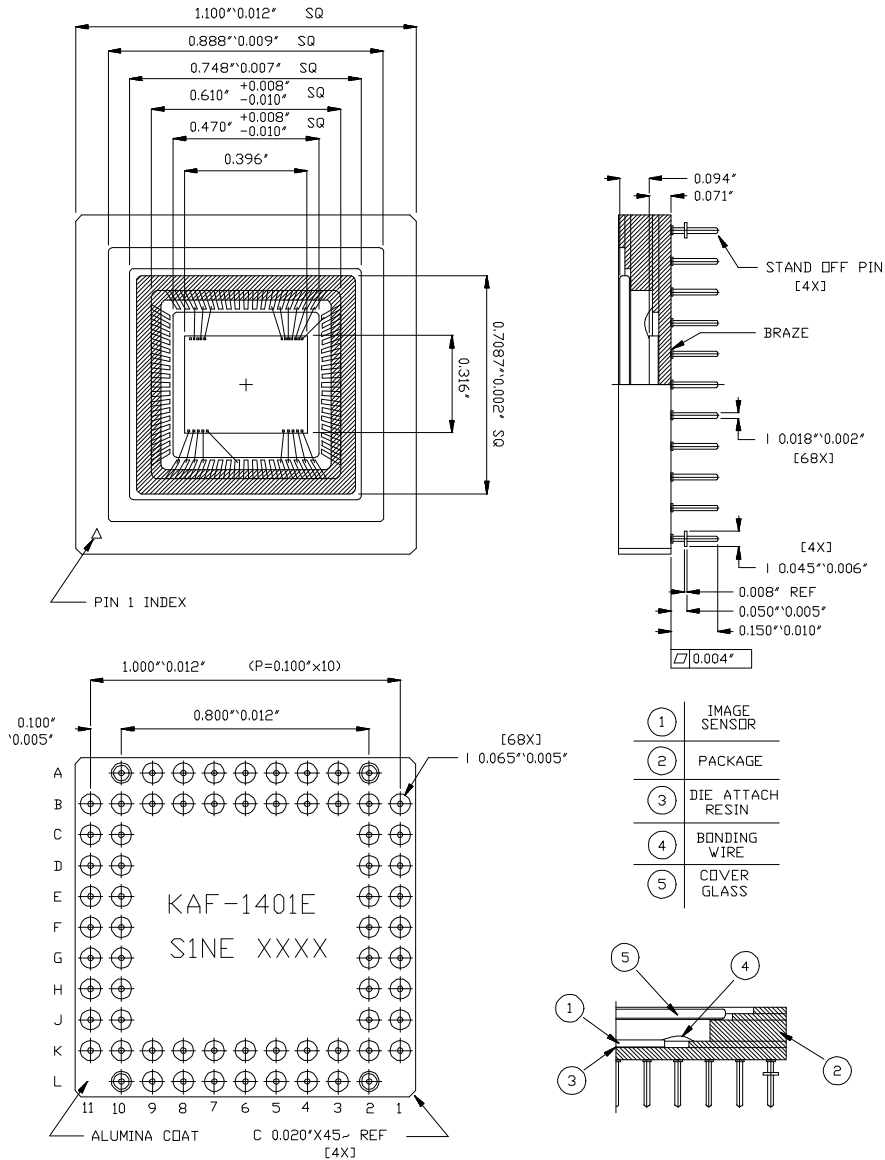


Figure 2 - Package Drawing



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2.2 Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1, 2	ϕV_1	Vertical CCD Clock - Phase 1	36	Vrd	Reset Drain
3, 4	ϕV_2	Vertical CCD Clock - Phase 2	37	Vss	Amplifier Return
8, 13, 49	Vsub	Substrate (Ground)	38	Vlg	Amplifier Load Gate
14, 15	ϕV_2	Vertical CCD Clock - Phase 2	39	Vout	Video Output
16, 17	ϕV_1	Vertical CCD Clock - Phase 1	40	Vdd	Amplifier Supply
34	Vog	Output Gate	47	ϕH_1	Horizontal CCD Clock - Phase 1
35	ϕR	Reset Clock	48	ϕH_2	Horizontal CCD Clock - Phase 2

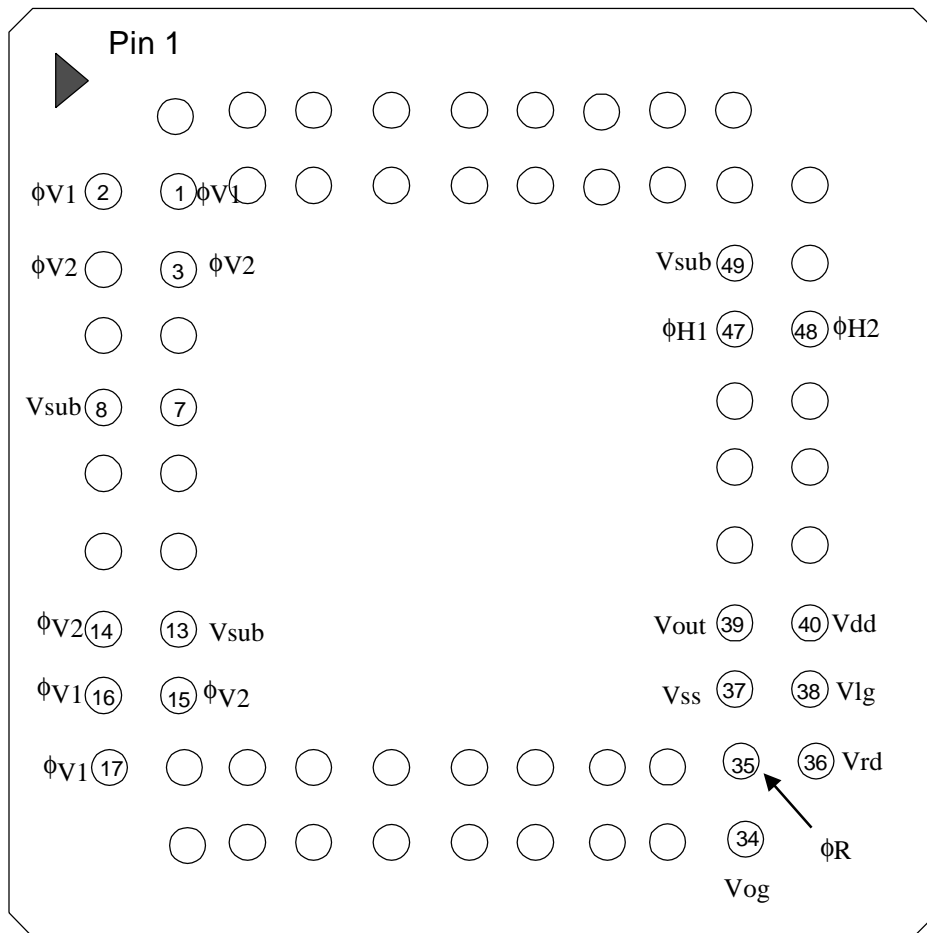


Figure 3 - Package Pin Assignment (Top View of Pin Grid Array)



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3.1 Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1, 2
Gate Pin Voltages - Type 1	Vgate1	-16	16	V	1, 3
Gate Pin Voltages - Type 2	Vgate2	0	16	V	1, 4
Inter-Gate Voltages	Vg-g		16	V	5
Output Bias Current	Iout		-10	mA	6
Output Load Capacitance	Cload		15	pF	6
Storage Temperature	T		100	°C	
Humidity	RH	5	90	%	7

Notes:

1. Referenced to pin Vsub.
2. Includes pins: Vrd, Vdd, Vss, Vout.
3. Includes pins: $\phi V1$, $\phi V2$, $\phi H1$, $\phi H2$, ϕR .
4. Includes pins: Vog, Vlg.
5. Voltage difference between overlapping gates. Includes: $\phi V1$ to $\phi V2$, $\phi H1$ to $\phi H2$, $\phi V2$ to $\phi H1$, $\phi H2$ to Vog.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. T=25°C. Excessive humidity will degrade MTTF.

CAUTION: This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for Class 1 devices.



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3.2 DC Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Max DC Current (mA)	Notes
Reset Drain	Vrd	11	11.5	11.75	V	0.01	
Output Amplifier Return	Vss	1.5	2.0	2.5	V	-0.5	
Output Amplifier Supply	Vdd	14.5	15	15.5	V	Iout	
Substrate	Vsub	0	0	0	V	0.01	
Output Gate	Vog	4.5	5	5.25	V	0.01	
Amplifier Load Gate	Vlg	Vss	Vss+1.0	Vss+1.5	V	0.01	
Video Output Current	Iout		-5	-10	mA	-	1

Notes:

1. An output load sink must be applied to Vout to activate output amplifier - see Figure below.

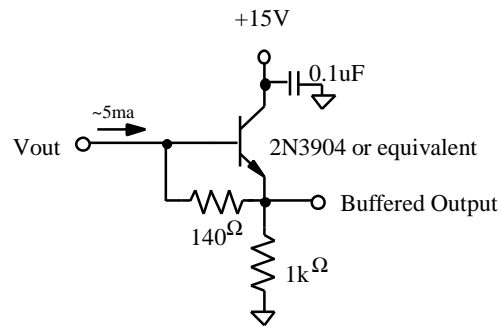


Figure 4 - Recommended Output Structure Load Diagram



3.3 AC Operating Condition

Description	Symbol	Level	Min.	Nom.	Max.	Units	Effective Capacitance
Vertical CCD Clock - Phase 1	$\phi V1$	Low	-10.5	-10.0	-9.5	V	24nF (all $\phi V1$ pins)
		High	-0.5	0	1.0	V	
Vertical CCD Clock - Phase 2	$\phi V2$	Low	-10.5	-10.0	-9.5	V	24nF (all $\phi V2$ pins)
		High	-0.5	0	1.0	V	
Horizontal CCD Clock - Phase 1	$\phi H1$	Low	-5.0	-4.0	-3.5	V	100pF
		High	5.0	6.0	6.5	V	
Horizontal CCD Clock - Phase 2	$\phi H2$	Low	-5.0	-4.0	-3.5	V	100pF
		High	5.0	6.0	6.5	V	
Reset Clock	ϕR	Low	-4.0	-3.0	-1.75	V	5pF
		High	3.5	4.0	5.0	V	

Notes:

- All pins draw less than 10uA DC current.
- Capacitance values relative to VSUB.

3.4 AC Timing Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Notes
$\phi H1, \phi H2$ Clock Frequency	f_H		10	15	MHz	1, 2, 3
$\phi V1, \phi V2$ Clock Frequency	f_V		71.5	101.6	kHz	1, 2, 3
Pixel Period (1 Count)	t_e	67	100		ns	
$\phi H1, \phi H2$ Setup Time	$t_{\phi HS}$	0.5	1		us	
$\phi V1, \phi V2$ Clock Pulse Width	$t_{\phi V}$	1.5	2		us	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	98.4	147		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	94.9	139.8		us	7

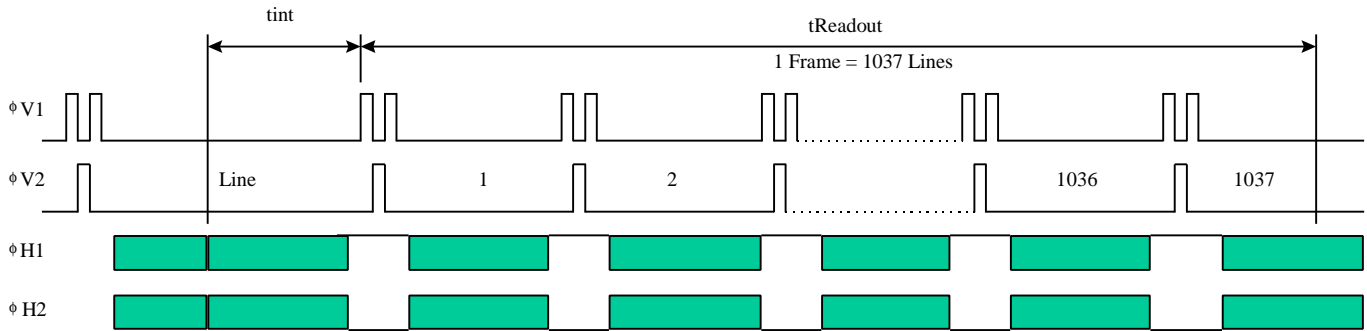
Notes:

- 50% duty cycle values.
- CTE may degrade above the nominal frequency.
- Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
- ϕR should be clocked continuously.
- $t_{readout} = (1037 * t_{line})$
- Integration time is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
- $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + (1348 * t_e) + t_e$

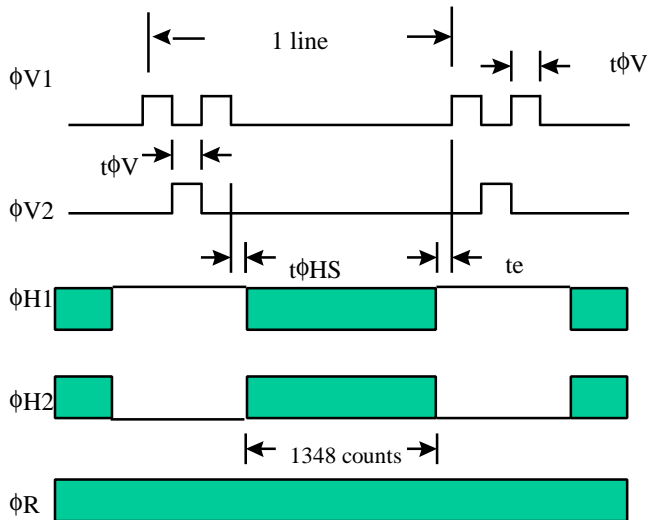


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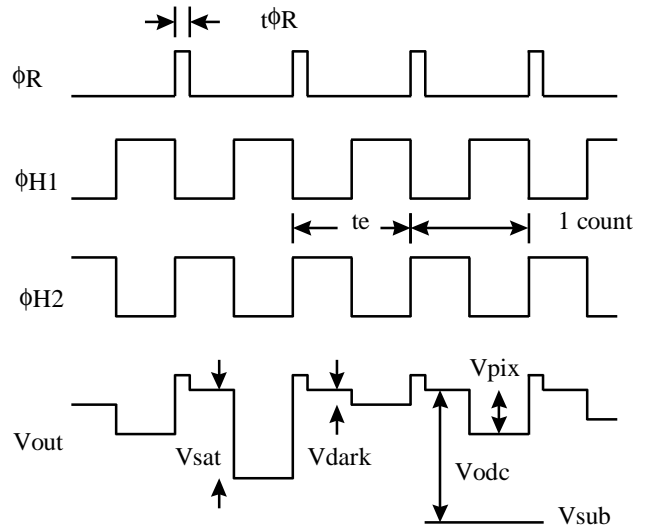
Frame Timing



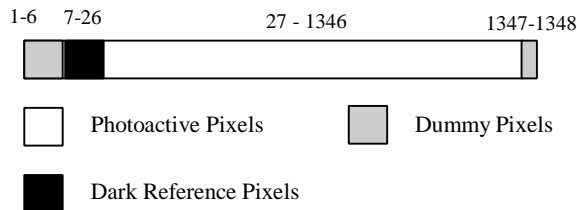
Line Timing Detail



Pixel Timing Detail



Line Content



- V_{sat} Saturated pixel video output signal
- V_{dark} Video output signal in no light situation, not zero due to J_{dark}
- V_{pix} Pixel video output signal level, more electrons = more negative
- V_{dc} Video level offset with respect to v_{sub}
- V_{sub} Analog Ground

* See Image Acquisition section (page 4)

Figure 5 - Timing Diagrams



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4.1 Performance Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation Signal						
Vertical CCD capacity	Nsat	40000	45000		electrons / pixel	1
Horizontal CCD capacity		90000	100000			
Output Node capacity		180000	200000	220000		
Red Quantum Efficiency ($\lambda=650\text{nm}$)	Rr	52	65	71	%	
Green Quantum Efficiency ($\lambda=550\text{nm}$)	Rg	42	52	57	%	
Blue Quantum Efficiency ($\lambda=450\text{nm}$)	Rb	32	40	44	%	
Blue Quantum Efficiency ($\lambda=400\text{nm}$)	Rb(400)	24	30	33	%	
Photoresponse Non-Linearity	PRNL		1	2	%	2
Photoresponse Non-Uniformity	PRNU		1	3	%	3
Dark Signal	Jdark		15	30	electrons / pixel / sec	4
			6	10	pA/cm ²	25°C
Dark Signal Doubling Temperature		5	6	7	°C	
Dark Signal Non-Uniformity	DSNU		15	30	electrons / pixel / sec	5
Dynamic Range	DR	67	72		dB	6
Charge Transfer Efficiency	CTE	0.99997	0.99999			
Output Amplifier DC Offset	Vodc	10.5	11.5	12.5	V	7
Output Amplifier Bandwidth	f _{-3dB}		45		Mhz	8
Output Amplifier Sensitivity	Vout/Ne~	9	11		uV/e~	
Output Amplifier output Impedance	Zout	175	200	250	Ohms	
Noise Floor	ne~		12	20	electrons	9

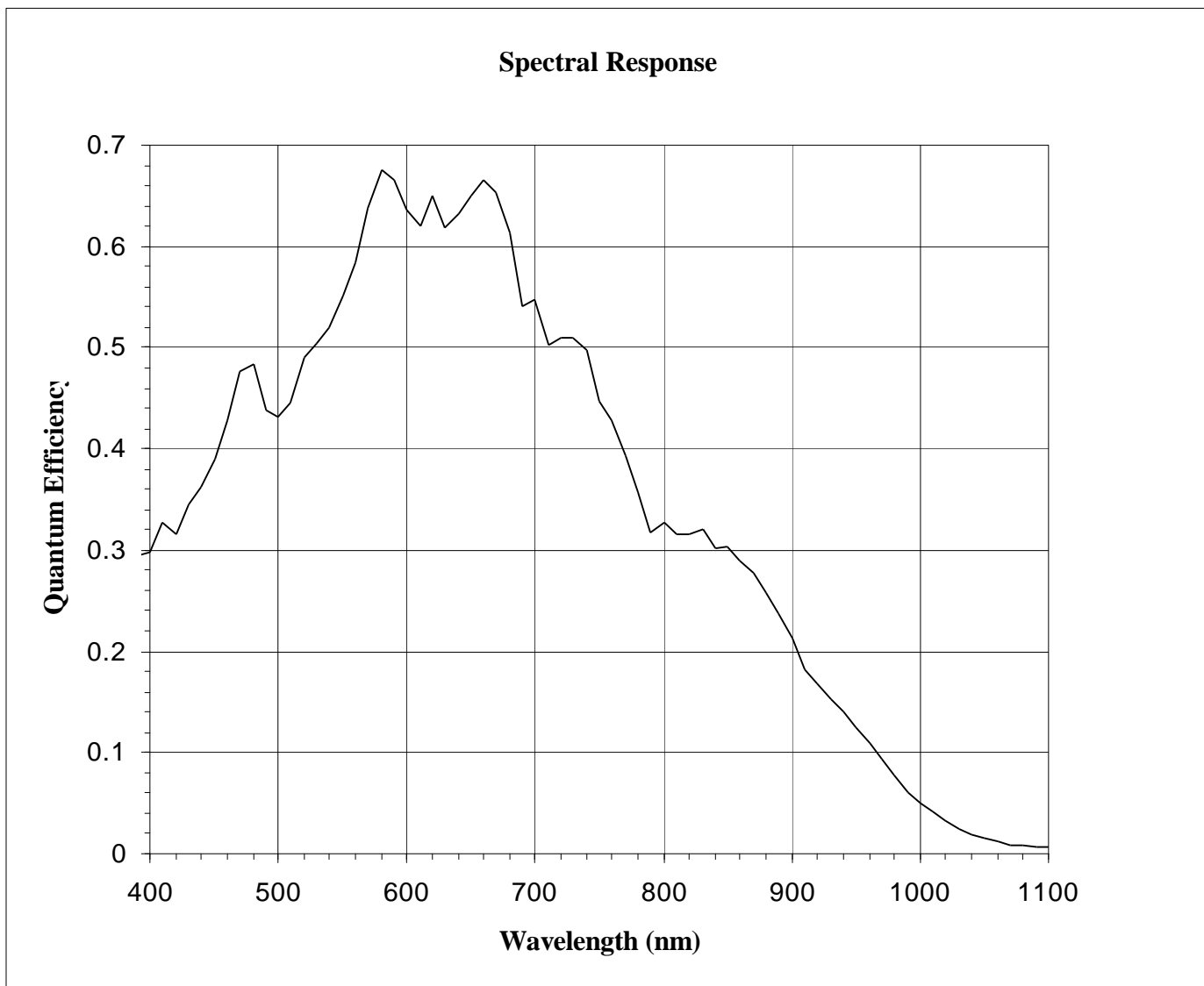
Notes:

- For pixel binning applications, electron capacity up to 330000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
- Worst case deviation from straight line fit, between 2% and 90% of Vsat.
- One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
- Average of all pixels with no illumination at 2 °C..
- Average dark signal of any of 11 x 8 blocks within the sensor. (each block is 128 x 128 pixels)
- $20\log (Nsat / ne\sim)$ at nominal operating frequency and 25°C.
- Video level offset with respect to ground (with Vrd = 11.0 volts)
- Last output amplifier stage only. Assumes 10pF off-chip load..
- Output noise at -10 °C , nominal operating frequency, and tint = 0 (excluding dark signal).



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4.2 Typical Performance Characteristics



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4.3 Cosmetic Grades

Defect tests performed at T=25°C

Standard

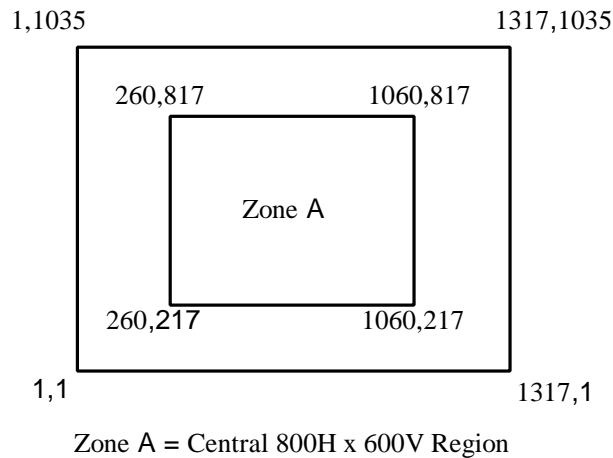
Class	Point Defects		Cluster Defects		Column Defects	
	Total	Zone A	Total	Zone A	Total	Zone A
C0	0	0	0	0	0	0
C1	≤5	≤2	0	0	0	0
C2	≤10	≤5	≤2	0	0	0
C3	≤20	≤10	≤4	≤4	≤4	≤2

UV Enhanced

UV	≤10	≤5	≤4	≤2	0	0	Note 1
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Note:

- Sensors with UV enhancement coating are available with the same cosmetic grade as uncoated Class 2.



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Point Defect	DARK: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR BRIGHT: A Pixel with dark current > 5000 e/pixel/sec at 25°C.
Cluster Defect	A grouping of not more than 5 adjacent point defects
Column Defect	1) A grouping of >5 contiguous point defects along a single column, 2) A column containing a pixel with dark current > 12,000e/pixel/sec (bright column) 3) A column that does not meet the minimum vertical CCD charge capacity (low charge capacity column) 4) A column which loses more than 250e under 2Ke illumination.(trap defect))
Neighboring pixels Defect Separation	The surrounding 128 x 128 pixels or ± 64 columns/rows. Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).



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5.1 Quality Assurance and Reliability

- 5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.
- 5.1.2 Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale.
- 5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.
- 5.1.4 ESD Precautions: Devices are shipped in a static-safe container and should only be handled at static-safe work stations.
- 5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Microelectronics Technology Division and can be supplied upon request.
- 5.1.6 Test Data Retention: Devices have an identifying number of traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

5.2 Ordering Information

See Appendix 1 for available part numbers

Address all inquiries and purchase orders to:

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Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.



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APPENDIX

Appendix 1 - Part Number Availability

Device	Part Number	Features
KAF-1401E	2H4376	Taped Clear Cover Glass, Class 0
KAF-1401E	2H4377	Taped Clear Cover Glass, Class 1
KAF-1401E	2H4378	Taped Clear Cover Glass, Class 2
KAF-1401E	2H4379	Taped Clear Cover Glass, Class 3
KAF-1401E	2H4380	Taped Cover Glass, Engineering Grade
KAF-1401E	2H4381	Taped Cover Glass, Engineering Grade
KAF-1401E	2H4382	Sealed Clear Cover Glass, Class 0
KAF-1401E	2H4383	Sealed Clear Cover Glass, Class 1
KAF-1401E	2H4384	Sealed Clear Cover Glass, Class 2
KAF-1401E	2H4385	Sealed Clear Cover Glass, Class 3
KAF-1401E	2H4386	Sealed Clear Cover Glass, Engineering Grade
KAF-1401E	2H4387	Sealed Clear Cover Glass, Mechanical Grade
KAF-1401E	2H4696	Lumogen Enhanced Sealed Quartz Cover Glass
KAF-1401E	2H4697	Lumogen Enhanced Taped Clear Cover Glass



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